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DECLARATION

I, Toshihiro TAKAHASHI , a national of Japan, c/o Asamura Patent Office of 331-340, New Ohtemachi Building, 2-1, Ohtemachi-2-chome, Chiyoda-ku, Tokyo, Japan do hereby solemnly and sincerely declare:-

1) THAT I am well acquainted with the Japanese language and English language, and

2) THAT the attached is a full, true, accurate and faithful translation into the English language made by me of Japanese Patent Application No. 8-244445

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 22nd day of November , 2001.

Toshihiro Takahashi

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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

[Scope of Claim for a Patent]

[Claim 1]

A method of fabricating a semiconductor device comprising the steps of:

(1) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(2) forming a trench having a predetermined depth at a predetermined position of the circuit formation surface of said semiconductor substrate so that a trench can be formed;

(3) oxidizing said trench portion formed in said semiconductor substrate;

(4) burying a buried insulating film into said trench so oxidized;

(5) removing said buried insulating film formed on said oxidation prevention film; and

(6) removing said oxidation prevention film formed on the circuit formation surface of said circuit substrate.

[Claim 2]

A method of fabricating a semiconductor device

comprising the steps of:

(1) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(2) forming a trench having a predetermined depth at a predetermined position of the circuit formation surface of said semiconductor substrate so that a trench can be formed;

(3) removing corner portions formed by said trench on the circuit formation surface of said semiconductor substrate;

(4) oxidizing said trench portion formed in said semiconductor substrate;

(5) burying a buried insulating film into said trench so oxidized;

(6) removing said buried insulating film formed on said oxidation prevention film; and

(7) removing said oxidation prevention film formed on the circuit formation surface of said circuit substrate.

[Claim 3]

A method of fabricating a semiconductor device comprising the steps of:

(1) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(2) forming a trench having a predetermined depth at a predetermined position of the circuit formation surface of said semiconductor substrate so

that a trench can be formed;

(3) oxidizing said trench portion formed in said semiconductor substrate;

(4) burying a buried insulating film into said trench so oxidized;

(5) removing said buried insulating film formed on said oxidation prevention film;

(6) oxidizing said semiconductor substrate after said buried insulating film formed on said oxidation prevention film is removed; and

(7) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

[Claim 4]

A method of fabricating a semiconductor device comprising the steps of:

(1) forming an oxidation prevention film on a circuit formation surface of a semiconductor substrate;

(2) forming a trench having a predetermined depth at a predetermined position of the circuit formation surface of said semiconductor substrate so that a trench can be formed;

(3) removing corner portions formed by said trench on the circuit formation surface of said semiconductor substrate;

(4) oxidizing said trench portion formed in said semiconductor substrate;

(5) burying a buried insulating film into said trench so oxidized;

(6) removing said buried insulating film formed on said oxidation prevention film;

(7) oxidizing said semiconductor substrate after said buried insulating film formed on said oxidation prevention film is removed; and

(8) removing said oxidation prevention film formed on the circuit formation surface of said semiconductor substrate.

[Claim 5]

A semiconductor device of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate is a trench isolation structure, characterized in that an angle θ of a trench, which constitutes said trench isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range of $90° < \theta < 180°$.

[Claim 6]

A semiconductor device of the type wherein a device isolation oxide film structure formed on a circuit formation surface of a semiconductor substrate is a trench isolation structure, characterized in that an angle θ of a trench, which constitutes said trench

isolation structure with the circuit formation surface of said semiconductor substrate, in a depth-wise direction with respect to the side surface of said semiconductor substrate is within the range of 90° < θ < 180°, and a silicon dioxide exists inside said trench.

[Detailed Description of the Invention]

[0001]

[Technical Field Pertinent to the Invention]

This invention relates to a semiconductor device having a trench isolation structure having high reliability, and a method of fabricating the same.

[0002]

[Prior Art]

An LOCOS (Local Oxidation of Silicon structure) is known as a structure for electrically insulating and isolating adjacent devices on a semiconductor substrate. This structure is formed by selectively oxidizing a substrate surface to form a thick thermal oxide film, and has been employed in various semiconductor devices. However, because this LOCOS structure has low processing accuracy, it is not suitable for an insulation/isolation structure of high integration semiconductor devices such as deep submicron devices in which high processing dimensional accuracy is required for the thermal oxide film. Therefore, a so-called "trench isolation structure" by a selective

oxidation method, which forms shallow trenches in the substrate surface and then selectively oxidizes the trench portions to form the thermal oxide film, has been employed in place of the LOCOS structure as the insulation/isolation structure of semiconductor devices for which high integration density is required, as described in JP-A-63-143835, for example.

[0003]

In comparison with the LOCOS structure, this trench isolation structure has the advantage that it can form device isolation oxide films having smaller planar dimensions. For this reason, this method is suitable for the fabrication of deep submicron devices for which processing dimensional accuracy of 0.5 μm or below is required.

[0004]

[Problem to be Solved by the Invention]

When a silicon thermal oxide film is formed by oxidizing the surface of a silicon substrate as a semiconductor substrate, for example, a large mechanical stress develops near the interface between the thermal oxide film so formed and the silicon substrate. This is because a part of the silicon substrate (Si) is oxidized and undergoes volume expansion of about twice when it changes to the thermal oxide film (SiO_2). When this mechanical stress increases, crystal defects such as dislocation and stacking faults are likely to occur and

reliability of the semiconductor devices drops. It has been also clarified that the oxidation reaction itself (diffusion behavior of oxidizing species, reactivity on the oxidation interface, etc) is affected by the stress and the shape of the growing oxide film changes. Since the stress occurs concentratedly near the end points (corner points) of the two-dimensional or three-dimensional shape, careful attention must be paid particularly to the crystal defects and the shape change in this stress concentration field.

[0005]

Fig. 1 is a schematic view of a fabrication process of a trench isolation structure in a conventional selective oxidation method. According to the conventional method shown in Fig. 1, an oxidation prevention film 3 is first deposited to a surface of a silicon substrate 1 through a pad oxide film (silicon thermal oxide film) 2, then the oxidation prevention film 3, the pad oxide film 2 and the silicon substrate 1 of the area, where a device isolation oxide film is desired to be formed, are partially removed to form a trench (Fig. 1(b)), and the silicon thermal oxide film 5 is formed by oxidizing the trench surface. In this trench isolation structure, the end points (corner points) essentially exist near the trench upper end portion or the trench lower end portion of the substrate. Therefore, the stress concentration field is

formed near the end point (corner point) due to thermal oxidation. Because such a stress concentration field is formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape 4 having an acute angle as shown in Fig. 1(c). After the formation of the device isolation oxide film, an electric circuit such as transistors, capacitors, etc, is formed in a device formation area covered with the oxide protective film 3 as shown in Fig. 1(d). If such an acute angle portion 4 remains on the substrate surface, however, the concentration of the electric field occurs at this portion during the circuit operation and deteriorates the breakdown voltage characteristics of the transistors, the capacitances, etc, that constitute the circuit, as pointed out by A. Bryant et al. In "Technical Digest of IEDM '94", pp. 671-674.

[0006]

In semiconductor devices having a trench isolation structure, the present invention is directed to provide a semiconductor device which does not invite deterioration of breakdown voltage characteristics of transistors and capacitances constituting a circuit but has high reliability, and a method of fabricating such a semiconductor device.

[0007]

[Means for Solving Problem]

The object described above can be accomplished by preventing a substrate shape in the proximity of the upper end portion of a device isolation trench on a surface of a semiconductor substrate from becoming an acute angle.

A method of fabricating a semiconductor device for accomplishing the object described above includes the following steps.

(1) Step to form oxide prevention film on circuit formation surface of a semiconductor substrate:

A silicon substrate, etc, may be used as the semiconductor substrate.

The film thickness of the oxidation prevention film must be such that all the oxide prevention films are not oxidized in the oxidation steps of the post-steps (4), (7), etc.

A polycrystalline silicon thin film, a silicon nitride film, etc, may be used as the oxidation prevention film. Since easily oxidizable materials such as the polycrystalline silicon thin film have low restriction force to volume expansion of the silicon substrate with oxidation, the stress concentration at the trench upper end portion can be reduced. Since difficultly oxidizable materials such as the silicon nitride film have a small oxidation quantity in the

oxidation process, the film thickness can be reduced.

[0008]

It is also effective to form a pad oxide film on the silicon substrate before the oxidation prevention film is formed. If the pad oxide film exists, the portions in the proximity of the lower end of the oxidation prevention film and the upper end of the semiconductor substrate that keep contact with the pad oxide film are sequentially oxidized from the trench end portion, and the so-called "bird's beak" is formed at the contact portion between the pad oxide film and the semiconductor substrate. As a result, the radius of curvature at the corners near the upper end of the semiconductor substrate is promoted.

[0009]

(2) Step to form trench having predetermined depth at desired positions of circuit formation surface of semiconductor substrate:

This trench can be formed by an ordinary lithography method using a photoresist and etching, for example.

[0010]

(3) Step to remove corners formed by trench on circuit formation surface of semiconductor substrate:

This step is not always necessary, but if the corners are removed by this step, the oxidation step (7) of the post-step becomes unnecessary in most cases.

[0011]

(4) Step to oxidize trench portion formed in semiconductor Substrate:

The trench portion is oxidized by several to dozens of nm by oxidation. Due to this oxidation, the bird's beak is grown at the trench portion and a radius of curvature is formed at the corners at the trench upper end portion.

[0012]

(5) Step to bury buried insulating film into oxidized trench:

Preferably, the material used as the buried insulating film is essentially an insulating material and has a low dielectric constant. For, if a material having a high dielectric constant is used, a coupling capacitance, which is formed when a wiring material is deposited on this insulating film at a post-step, becomes great. From this aspect, a silicon oxide film, etc, is a preferred burying material, and polycrystalline silicon or the like is not preferred.

[0013]

(6) Step to remove buried insulating film formed on oxidation prevention film:

The buried insulating film is etched back by chemical-mechanical polishing (CMP) or dry etching. In this case, the oxidation prevention film serves as an etching stopper and has also the function of preventing

etching of the semiconductor substrate below the oxidation prevention film.

[0014]

(7) Step to oxidize semiconductor substrate after removal of buried insulating film formed on oxidation prevention film:

This step grows the radius of curvature of the trench upper end portion of the semiconductor substrate to a sufficient radius of curvature for preventing the increase of the leakage current. This oxidation step provides also the effect that the buried insulating film is made compact.

This step is not necessary if the radius of curvature at the trench upper end portion of the semiconductor substrate has become sufficient to prevent the increase of the leakage current due to the oxidation step (4).

This step may be executed before the step (6) or after the next step (8). When this step is executed after the next step (8), the surface of the semiconductor substrate is simultaneously oxidized, too, but the oxide film formed on the surface of the semiconductor substrate is removed after completion of additional oxidation and in this way, the step of forming the device isolation film is completed.

[0015]

(8) Step to remove oxidation prevention film formed on circuit formation surface of semiconductor substrate:

The formation step of the device isolation oxide film is completed by this step. Therefore, a semiconductor device is formed by forming a circuit such as transistors on the semiconductor substrate on which the device isolation oxide film is formed.

[0016]

A semiconductor device according to the present invention for accomplishing the afore-mentioned objects is a semiconductor device having a device isolation oxide film which is formed on a circuit formation surface of a semiconductor substrate and is a trench isolation structure, wherein an angle θ between the circuit formation surface of the semiconductor substrate and the side surface of the semiconductor substrate in a depth-wise direction of the trench constituting the trench isolation structure is within the range of $90° < \theta < 180°$. Because this structure can prevent field concentration at the trench u-per end portion, it can prevent the increase of a leakage current resulting from deterioration if breakdown voltage characteristics of the circuit such as transistors and capacitances formed on the semiconductor substrate.

[0017]

The coupling capacitance of wiring constituted on the semiconductor substrate can be reduced by burying the inside of the trench by an insulating material having a low dielectric constant such as a silicon oxide, and reliability of the semiconductor device can be further improved.

[0018]

[Mode for Carrying Out the Invention]

Hereinafter, preferred embodiments of the present invention will be explained with reference to the accompanying drawings.

[0019]

[Embodiment]

A fabrication process of an MOS transistor according to the first embodiment of the present invention will be explained with reference to Figs. 2 and 3. Fig. 2 is a schematic view of the fabrication process of the MOS transistor according to the first embodiment and Fig. 3 is a flowchart of the fabrication process of the MOS transistor according to the first embodiment.

[0020]

The fabrication process of the MOS transistor of this first embodiment is as follows.

(1) A surface of a silicon substrate 1 is thermally oxidized so as to form a pad oxide film 2

having a thickness of 10 to several tens of nm [Fig. 3 (101) to (102)].

[0021]

(2) A polycrystalline silicon thin film 18 is deposited on the pad oxide film 2 to a thickness of about 10 to 200 nm [Fig. 3 (103)]. This polycrystalline silicon thin film 18 is used as an oxidation prevention film when a device isolation thermal oxide film 5 is formed. Incidentally, the polycrystalline silicon film 18 may be directly deposited on the silicon substrate 1 by omitting the formation of the pad oxide film 2.

Incidentally, the following description is based on the assumption that the pad oxide film 2 is formed. Therefore, the process step relating to the pad oxide film 2 is not necessary when the formation of the pad oxide film 2 is omitted.

[0022]

(3) A photoresist 19 is formed on the polycrystalline silicon film 18 [Fig. 2(b), Fig. 3 (104)].

[0023]

(4) After the photoresist 19 in an area, in which a device isolation film is to be formed, is removed by an ordinary lithography method, a part each of the polycrystalline silicon thin film 18, the pad oxide film 2 and the silicon substrate 1 is removed by etching so as to form a shallow trench whose side walls have a predetermined angle (substantially, about 60 to about 90

degrees) on the surface of the silicon substrate 1 [Figs. 2(c) to 2(d), Fig. 3 (105 to (107))].

[0024]

(5) After the photoresist 19 is removed, thermal oxidation is carried out so as to oxidize the trench portion formed in the surface of the silicon substrate 1 to several to dozens of nm [Figs. 2(e) and 2(f), Fig. 3 (108) to (109)]. Incidentally, a sufficient film thickness of the polycrystalline silicon thin film 18 deposited as the oxidation prevention film must be secured so that it can function as the oxidation prevention film for preventing the polysilicon film 18 from being fully oxidized at the time of thermal oxidation and preventing the silicon substrate 1 below this polycrystalline silicon thin film 18 from being oxidized entirely. At this time, the surface of the polycrystalline silicon thin film 18 is oxidized, too. When this pad oxide film 2 exists, silicon in the proximity of the lower end of the polycrystalline silicon thin film 18 and the upper end of the silicon substrate 1 keeping contact with the pad oxide film 2 is sequentially oxidized from the trench end, and a so-called "bird's beak" is formed between the contact portions. As a result, the radius of curvature in the proximity of the upper end of the silicon substrate 1 is promoted. From this aspect, the pad oxide film 2 is preferably formed.

[0025]

(6) Because the inside of the trench is not completely buried by this trench oxidation, an insulating film 9 such as a silicon oxide film is deposited by chemical vapor deposition, sputtering, etc, in order to completely bury the inside of the trench covered by the thermal oxidation film (hereinafter, the insulating film 9 for burying the inside of the trench will be called the "buried insulating film 9") [Fig. 2 (g), Fig. 3 (110)]. Basically, the material used for this buried insulating film 9 is an insulating material and preferably has a low dielectric constant. For, when a material having a high dielectric constant is used, a coupling capacitance formed when a wiring material is deposited on this film in a post-step becomes greater. From this aspect, it is not preferred to use polycrystalline silicon as the burying material.

[0026]

(7) The buried insulating film 9 is then etched back by chemical-mechanical polishing (CMP) or dry etching [Fig. 2(g), Fig. 3(111)]. In this case, the polycrystalline silicon thin film 18 used as the oxidation prevention film functions as an etching stopper and plays the role of preventing the silicon substrate 1 below the polycrystalline silicon thin film 18 from being etched.

[0027]

(8) When the radius of curvature of the trench upper end portion due to the bird's beak grown between the contact portions by the oxidation of the trench portion of the silicon substrate 1 is sufficient for preventing the increase of the leakage current, the formation step of the device isolation oxide film is completed by removing the polycrystalline silicon thin film 18 and the pad oxide film 2 [Figs. 2(h), (i), Fig. 3 (113)].

[0028]

When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate 1 is not sufficient for preventing the leakage current depending on the product specification for each product, for example, thermal oxidation is again carried out (hereinafter called "additional oxidation") after the buried insulating film 9 is etched back from the next product lot [Fig. 2(l), Fig. 3(112)].

[0029]

In this case, since the buried insulating film 8 has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from near the trench upper end portion 12 and the inside of the trench is hardly oxidized for the following reason. In other words, though the inside of the trench is to be

thermally oxidized through the buried insulating film 9, a longer time is necessary for the oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially within a short period of several minutes near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench side walls and the upper surface of the trench exists at the trench upper end portion 12, and the oxidation seeds can diffuse at a relatively high rate along this weak boundary layer. As a result, the oxidation seeds are supplied to the trench upper end portion 12 within a short time (10 or more minutes at the oxidation temperature of 850°C), so that only the portions in the proximity of the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature of the trench upper end portion 12 is promoted.

[0030]

Furthermore, this additional oxidation provides the effect of rendering the buried insulating film 9 compact. After this additional oxidation is completed, the formation step of the device isolation oxide film is completed by removing the polycrystalline silicon thin film 18 and the pad oxide film 2

[Fig. 2(m), Fig. 3 (113)].

[0031]

This additional oxidation may be carried out after the polycrystalline silicon thin film 18 is removed. In this case, the surface of the silicon substrate 1 is simultaneously oxidized, too, but the formation step of the device isolation oxide film is completed by removing this oxide film formed on the surface of the silicon substrate 1 after the additional oxidation is completed.

[0032]

(9) Transistor structures, etc, are formed on the silicon substrate 1 [Figs. 2(j), (h), Fig. 3 (114) to (122)].

Conventional fabrication technologies of the transistor structure, etc, can be employed without particular limitation, and a typical fabrication process of the MOS transistor structure will be explained next by way of example.

[0033]

(a) Any of a silicon oxide film, a silicon nitride film, an acid nitride film and a high dielectric thin film, or their laminate body, is formed as the gate oxide film 6 on the silicon substrate 1.

These thin films can be formed by CVD, or the like, for example. The silicon oxide film may be formed by thermal oxidation of the silicon substrate 1.

[0034]

(b) Any of a polycrystalline silicon thin film, a metal thin film such as a tungsten film and a silicide thin film, or their laminate body, is formed and then unnecessary portions are removed by etching, etc, to form a gate electrode 7.

[0035]

(C) An impurity is implanted and a first layer within 10, an inter-layer insulating film 11, etc, are formed.

The MOS transistor described above can be used for memory circuits such as a DRAM (Dynamic Random Access Memory) or arithmetic operation circuits such as logic devices.

[0036]

The first embodiment described above can prevent the acute angle portions from remaining near the trench upper end portions of the silicon substrate when the trench isolation structure is formed as the device isolation oxide film structure, can prevent the increase of the leakage current or the drop of withstand voltage characteristics of the MOS transistor resulting from the field concentration in the proximity of the gate electrode film, by forming the radius portions or the obtuse angle portions near the trench upper end portion of the silicon substrate, and can improve electrical reliability of the transistor.

[0037]

Incidentally, since the trench upper end portion of the silicon substrate before thermal oxidation is substantially orthogonal in the first embodiment, there is the case where the radius of curvature near the trench upper end portion of the silicon substrate is not sufficient. However, because polycrystalline silicon as the oxidation prevention film is easily oxidized, the restriction force to the volume expansion of the silicon substrate is lower in comparison with those materials which are difficultly oxidized, and there is sometimes the case where additional oxidation is not necessary. Furthermore, processing of the trench is easy and this embodiment is excellent in the aspect of productivity, too.

[0038]

Next, the fabrication process of an MOS transistor according to the second embodiment of the present invention will be explained with reference to Figs. 4 and 5. Fig. 4 is a schematic view showing the fabrication process of the MOS transistor according to the second embodiment and Fig. 5 is a flowchart of the fabrication process of the MOS transistor of this embodiment.

[0039]

The fabrication process of the MOS transistor of the second embodiment modifies the fabrication

step (4) of the first embodiment in the following way. Since the fabrication steps other than the step (4) are the same as those of the first embodiment, the detailed explanation will be omitted.

[0040]

(4) After the photoresist 19 of the area in which the device isolation film is to be formed is removed by an ordinary exposure method, a part of each of the polycrystalline silicon thin film 18, the pad oxide film 2 and the silicon substrate 1 is removed by etching, and a shallow trench is formed in the surface of the silicon substrate 1. When forming the trench in the surface of the silicon substrate, isotropic etching is applied near the trench upper end portion so as to form the radius of curvature near the trench upper end portion, and then anisotropic etching is applied so as to define the trench shape having the slope portion like the isotropic etching portion 13. Incidentally, the angle of the trench side walls near the trench lower end portion need not always be 90 degrees and a predetermined inclination (substantially within the range of 60 to 90 degrees) [Figs. 4(c) to (e), Fig. 5 (205) to (207)] may be formed.

[0041]

In comparison with the second embodiment, etching step at the time of formation of the shallow trench becomes more complicated. However, because the

isotropic etching portion 13 is disposed at the trench upper end portion of the silicon substrate at the time of formation of the shallow trench as described above, oxidation of the trench upper end portion of the silicon substrate 1 by first thermal oxidation is promoted, and the necessity for additional oxidation becomes lower.

[0042]

Next, the fabrication process of an MOS transistor according to the third embodiment of the present invention will be explained with reference to Figs. 6 and 7. Fig. 6 is a schematic view of the fabrication process of the MOS transistor according to the third embodiment and Fig. 7 is a flowchart of the fabrication process of the MOS transistor of the third embodiment.

[0043]

The fabrication process of the MOS transistor according to the third embodiment is as follows.

(1) The surface of the silicon substrate 1 is thermally oxidized and the pad oxide film 2 having a thickness of 10 to dozens of nm is formed [Fig. 7 (301) to (302)].

[0044]

(2) A silicon nitride film 17 having high oxidation resistance is deposited to a thickness of 10 to 200 nm on the pad oxide film 2 [Fig. 7 (103)]. This silicon nitride film 17 is used as an oxidation

prevention film when the device isolation oxide film 5 is formed. Incidentally, the silicon nitride film 17 having high oxidation resistance may be directly formed on the silicon substrate 1 by omitting the formation of the pad oxide film 2. Alternatively, the silicon nitride film 17 is deposited through the pad oxide film 2 and the polycrystalline silicon thin film, or through only the polycrystalline silicon thin film. In either case, the silicon nitride film 17 exists on the outermost surface of the structure.

[0045]

Incidentally, the following description is based on the assumption that the polycrystalline silicon thin film and the pad oxide film 2 are formed. Therefore, when the formation of the polycrystalline silicon thin film and the pad oxide film 2 is omitted, the process steps relating to the polycrystalline silicon thin film and the pad oxide film 2 are not necessary.

[0046]

(3) The photoresist 19 is formed on the silicon nitride film 17 [Fig. 6(b), Fig. 7 (304)].

[0047]

(4) After the photoresist 19 of the area, in which the device isolation film is to be formed, is removed by an ordinary lithography method, the silicon nitride film 17, the pad oxide film 2 and the polycrystalline

silicon film are removed by etching. Next, the photoresist is removed, and the shallow trench is formed in the surface of the silicon substrate 1 by dry etching. When this trench is formed in the surface of the silicon substrate, isotropic etching is applied to the portions near the trench end portion so as to form the radius of curvature in the proximity of the trench upper end and then anisotropic etching is applied to form the trench shape having the slope portion like the isotropic etching portion 13. Incidentally, the angle of the trench side walls near the trench lower end portion need not always be 90 degrees, and a predetermined inclination (substantially within the range of 60 to 90 degrees) may be formed, as well [Figs. 6(c) to (e), Fig. 7 (305) to (308)].

[0048]

(5) After the photoresist 9 is removed, thermal oxidation is carried out to oxidize the trench portion formed in the surface of the silicon substrate 1 to a thickness of several to dozens of nm [Figs. 6(e) to (f), Fig. 7 (309)]. Incidentally, the film thickness of the silicon nitride film 17 as the oxidation prevention film must be a film thickness sufficient to function as the oxidation prevention film to prevent the silicon nitride film 17 from being completely oxidized at the time of thermal oxidation and to prevent the silicon substrate 1 below the silicon nitride film 17 from being completely

oxidized. Since this silicon nitride film 17 has high oxidation resistance, the film thickness can be made thinner than the polycrystalline silicon thin film 18 used in the first and second embodiments. When the pad oxide film 2 exists, silicon in the proximity of the upper end portion of the silicon substrate 1 keeping contact with the pad oxide film 2 and the lower end of the polycrystalline thin film are serially oxidized from the trench end, and the so-called "bird's beak" is formed, so that the radius of curvature near the upper end of the silicon substrate 1 is promoted. From this aspect, the pad oxide film 1 is preferably formed.

[0049]

(6) Since the inside of the trench is not fully buried by this trench oxidation, the insulating film 9 such as a silicon oxide film is deposited to bury the inside of the trench by chemical vapor deposition, sputtering, etc, in order to fully bury the inside of the trench covered by the thermal oxidation film (hereinafter, the insulating film 9 for burying the inside of the trench will be called the "buried insulating film 9") [Fig. 6(g), Fig. 7 (310)]. The material used for the burying insulating film 9 is preferably a material having an insulating property and a low dielectric constant. For, when a material having a high dielectric constant is used, a coupling capacitance formed when a wiring material is deposited

on the film material in the post-process becomes great. From this aspect, the use of polycrystalline silicon as the burying material is not preferred.

[0050]

(7) When the radius of curvature at the trench upper end portion due to the bird's beak grown by oxidation of the trench portion of the silicon substrate 1 is sufficient to prevent the increase of the leakage current, the formation process of the device isolation oxide film is completed by etching back the buried insulating film 9 and by removing the remaining silicon nitride film 17, polycrystalline silicon and the pad oxide film 2 [Figs. 6(h), (I), Fig. 7(313)].

[0051]

When the radius of curvature of the trench upper end portion due to the bird's beak grown by the oxidation of the trench portion of the silicon sub-strate 1 is not sufficient for preventing the increase of the leakage current, thermal oxidation is again carried out (hereinafter called "additional oxidation") before the buried insulating film 9 is etched back [Fig. 6(l), Fig. 7 (312)].

[0052]

In this case, since the buried insulating film 9 has already been formed inside the trench of the silicon substrate 1, oxidation proceeds from portions near the trench upper end portion 12 and the inside of

the trench is hardly oxidized for the following reason.

[0053]

In other words, thermal oxidation inside the trench is carried out through the buried insulating film 9 but in this case, a longer time is necessary for the oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 than when the silicon substrate is directly oxidized. Therefore, oxidation does not substantially proceed within a short time of several minutes near the bottom of the trench. On the other hand, a weak boundary layer of the coupling portion of the buried insulating film 9 deposited to the trench side walls and the trench upper surface by chemical vapor deposition or sputtering exists at the trench upper end portion 12. Accordingly, the oxidation seeds can diffuse at a relatively high rate along this weak boundary layer, so that the oxidation seeds are supplied to the trench upper end portion 12 within a short time (10 minutes or more at an oxidation temperature of 850°C), the portions near the trench upper end portion 12 are oxidized and the formation of the radius of curvature of the trench upper end portion 12 is promoted.

[0054]

When the radius of curvature of the trench upper end portion 12 due to the bird's beak grown by this additional oxidation is sufficient to prevent the

increase of the leakage current, the formation process of the device isolation oxide film is completed by etching back the buried insulating film 9 and then removing the remaining silicon nitride film 17, polycrystalline silicon and pad oxide film 2 [Fig. 6(m), Fig. 7 (313)].

Incidentally, this additional oxidation need not always be carried out before etch-back of the buried insulating film 9, and may be carried out after etch-back of the buried insulating film 9 in the same way as in the first embodiment.

[0055]

(8) A transistor structure, etc, is formed on the silicon substrate 1 [Figs. 6(j) to (n), Fig. 7 (314) to (322)].

Conventional fabrication technologies of the transistors can be employed without particular limitation, and the explanation will be given on a typical fabrication process of the MOS transistor structure by way of example.

[0056]

(a) Any of a silicon oxide film, a silicon nitride film, an acid nitride film and a high dielectric thin film, or their laminate body, is formed as the gate oxide film 6 on the silicon substrate 1.

These thin films can be formed by CVD, for example. The silicon oxide film may be formed by the

thermal oxidation of the silicon substrate 1.

[0057]

(b) After any of a polycrystalline silicon thin film, a metal film such as a tungsten film and a silicide thin film, or their laminate body, is formed, unnecessary portions are removed by etching, etc, to form the gate electrode 7.

[0058]

(c) An impurity is implanted and a first layer wiring 10, an inter-layer insulating film 11, etc, are formed. Wiring of the second layer et seq, and an insulating film are formed further, whenever necessary.

[0059]

The MOS transistor described above can be used for memory circuits such as a DRAM (Dynamic Random Access Memory), and SRAM (Static Random Access Memory) or arithmetic operation circuits such as logic devices, etc.

[0060]

In the fabrication process of the MOS transistor, the third embodiment prevents the acute angle portions from remaining in the proximity of the trench upper end portion of the silicon substrate when forming the trench isolation structure as the device isolation oxide film structure, but forms the radius of curvature portion or the obtuse angle portion near the trench upper end portion of the silicon substrate.

Therefore, this embodiment can prevent the increase of the leakage current of the MOS transistor or the drop of the breakdown voltage characteristics resulting from the field concentration near the end portion of the gate electrode, and can improve electrical reliability of the transistor.

[0061]

Incidentally, since the third embodiment uses the silicon nitride film 17 having high oxidation resistance as the oxidation prevention film, the film thickness of the oxidation prevention film can be reduced, and removal of this oxidation prevention film in the final process step becomes easier.

[0062]

The etching process at the time of the formation of the shallow trench gets complicated in this third embodiment in the same way as in the second embodiment but because the isotropic etching portion 13 is deposited at the trench upper end portion of the silicon substrate 1 when the shallow trench is formed as described above, oxidation of the trench upper end portion of the silicon substrate 1 is promoted in the initial thermal oxidation process and the necessity for additional oxidation becomes lower.

[0063]

Next, the fabrication process of an MOS transistor according to the fourth embodiment of the

present invention will be explained with reference to Figs. 8 and 9. Fig. 8 is a schematic view of the fabrication process of the MOS transistor of the fourth embodiment and Fig. 9 is a flowchart of the fabrication process of the MOS transistor in the third embodiment.

[0064]

(4) After the photoresist in the area in which the device isolation film is to be formed is removed by an ordinary lithography method, the silicon nitride film 17, the pad oxide film 2 and the polycrystalline silicon thin film are removed by etching. Next, the photoresist is removed and the shallow trench is formed in the surface of the silicon substrate 1 by dry etching. The angle of the trench side walls near the trench lower end portion need not always be 90 degrees and a predetermined inclination (substantially within the range of 60 to 90 degrees) may be formed [Figs. 8(c) to (e), Fig. 9 (405) to (408)].

[0065]

Since the fourth embodiment uses the silicon nitride film 17 having high oxidation resistance as the oxidation prevention film in the same way as in the third embodiment, the film thickness of the oxidation prevention film can be reduced, and removal of the oxidation prevention film in the final process step becomes easier.

The fourth embodiment can easily form the

trench has high productivity.

[0066]

[Effects of the Invention]

In the semiconductor devices having the trench isolation structure, the present invention can provide a semiconductor device which does not invite deterioration of the transistors constituting the circuit and the breakdown voltage characteristics of the capacitance, and a method of fabricating the semiconductor device.

[Brief Description of Drawings]

[Fig. 1]

Fig. 1 is a schematic view showing a fabrication process of a trench isolation structure in a selective oxidation method according to the prior art.

[Fig. 2]

Fig. 2 is a schematic view showing a fabrication process of an MOS transistor according to the first embodiment of the present invention.

[Fig. 3]

Fig. 3 is a flowchart showing the fabrication process of the MOS transistor according to the first embodiment of the present invention.

[Fig. 4]

Fig. 4 is a schematic view showing a fabrication process of an MOS transistor according to

the second embodiment of the present invention.

[Fig. 5]

Fig. 5 is a flowchart showing the fabrication process of the MOS transistor according to the second embodiment of the present invention.

[Fig. 6]

Fig. 6 is a schematic view showing a fabrication process of an MOS transistor according to the third embodiment of the present invention.

[Fig. 7]

Fig. 7 is a flowchart of the fabrication process of the MOS transistor according to the third embodiment of the present invention.

[Fig. 8]

Fig. 8 is a schematic view showing a fabrication process of an MOS transistor according to the fourth embodiment of the present invention.

[Fig. 9]

Fig. 9 is a flowchart of the fabrication process of the MOS transistor according to the fourth embodiment of the present invention.

[Description of Reference Numerals]

1 ... silicon substrate

2 ... pad oxide film

6 ... gate oxide film

9 ... buried insulating film

12 ... trench upper end portion

13 ... isotropic etching portion

17 ... silicon nitride film

18 ... polycrystalline silicon film

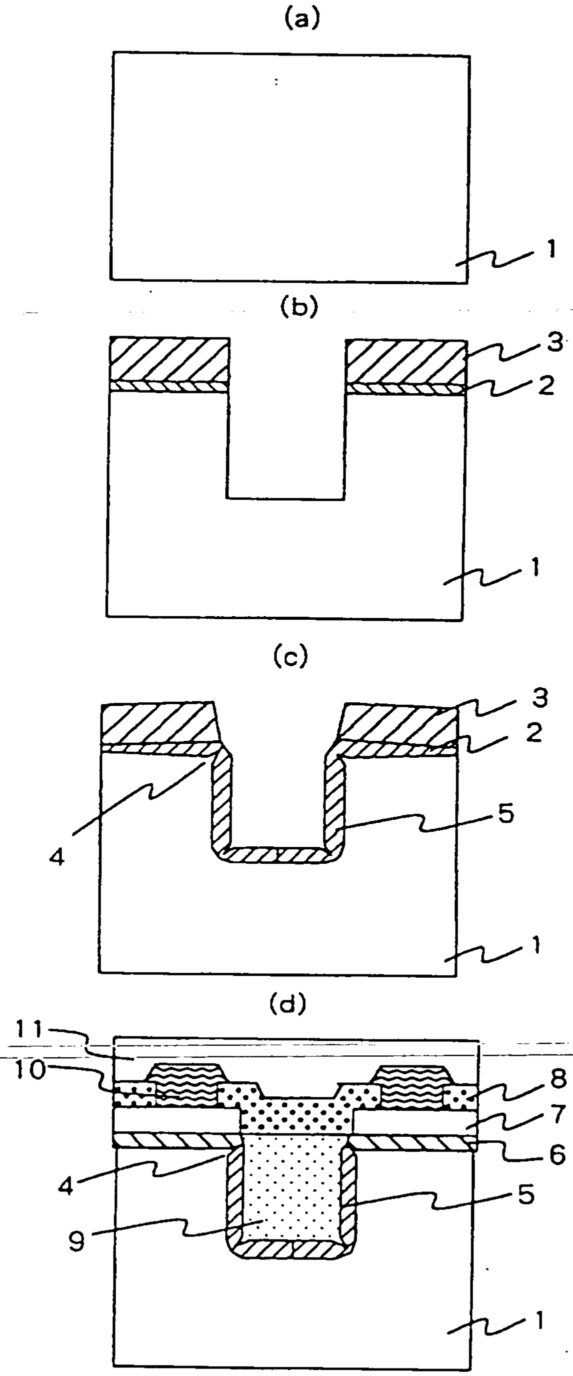
19 ... photoresist

【書類名】 図面 [Title of Document] Drawings

【図1】 [Fig.1]

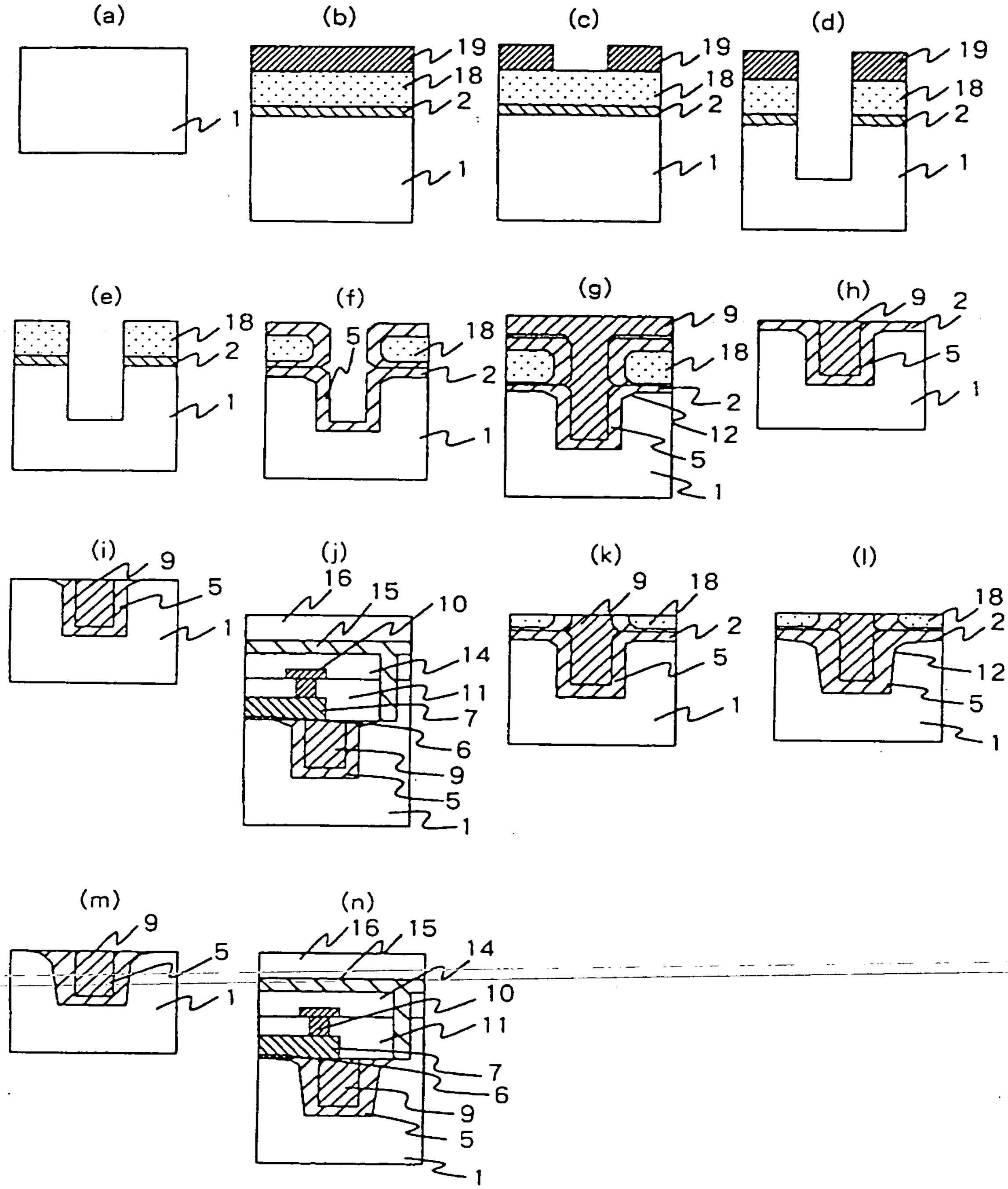
Fig. 1

図 1



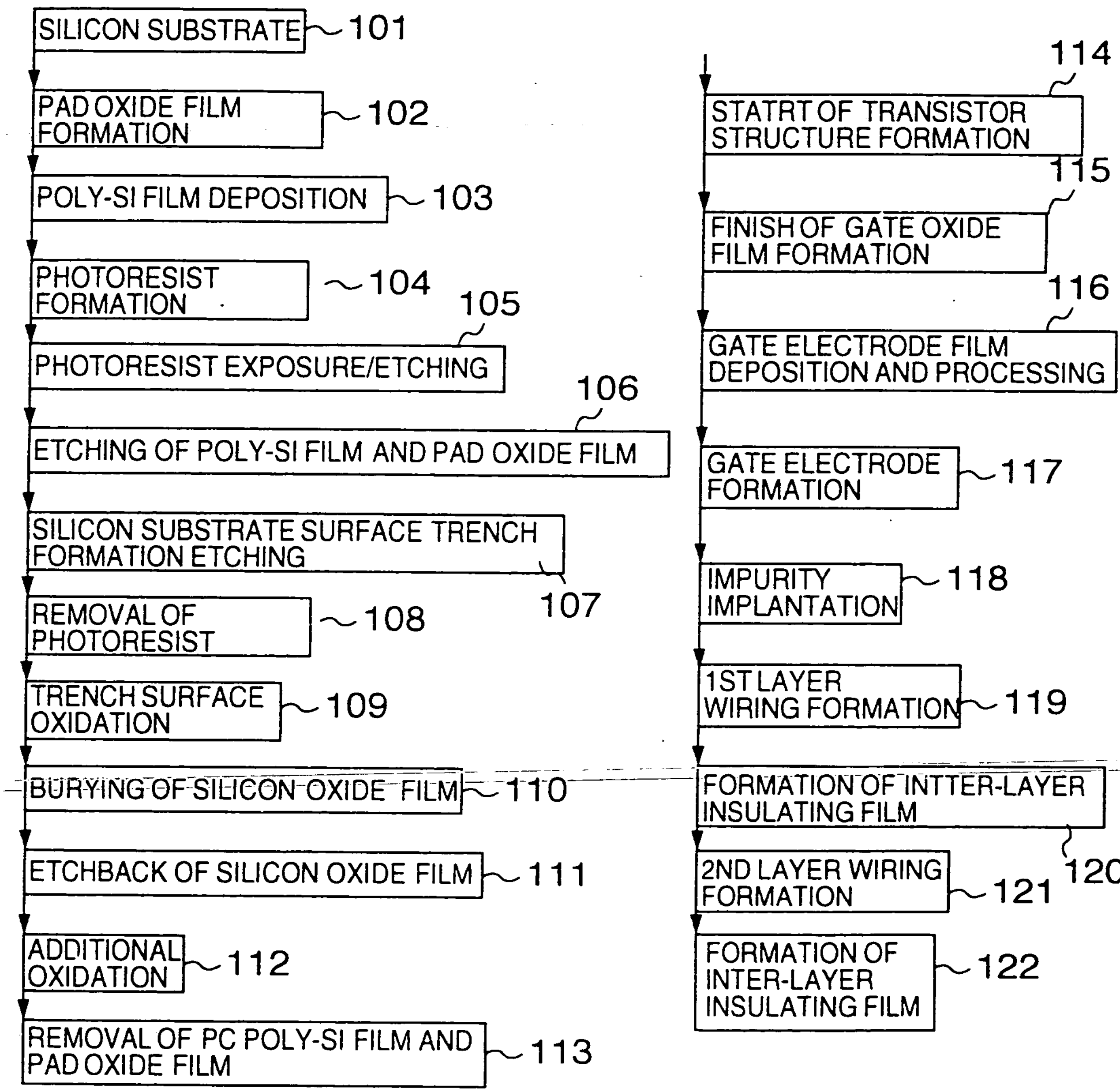
【図2】 [Fig.2]

Fig.2
図 2



[Fig. 3]

FIG. 3



SILICON SUBSTRATE
101
PAD OXIDE FILM FORMATION
102
POLY-SI FILM DEPOSITION
103
PHOTORESIST FORMATION
104
PHOTORESIST EXPOSURE/ETCHING
105
ETCHING OF POLY-SI FILM AND PAD OXIDE FILM
106
SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING
107
REMOVAL OF PHOTORESIST
108
TRENCH SURFACE OXIDATION
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BURYING OF SILICON OXIDE FILM
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ETCHBACK OF SILICON OXIDE FILM
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FINISH OF GATE OXIDE FILM FORMATION
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GATE ELECTRODE FILM DEPOSITION AND PROCESSING
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2ND LAYER WIRING FORMATION
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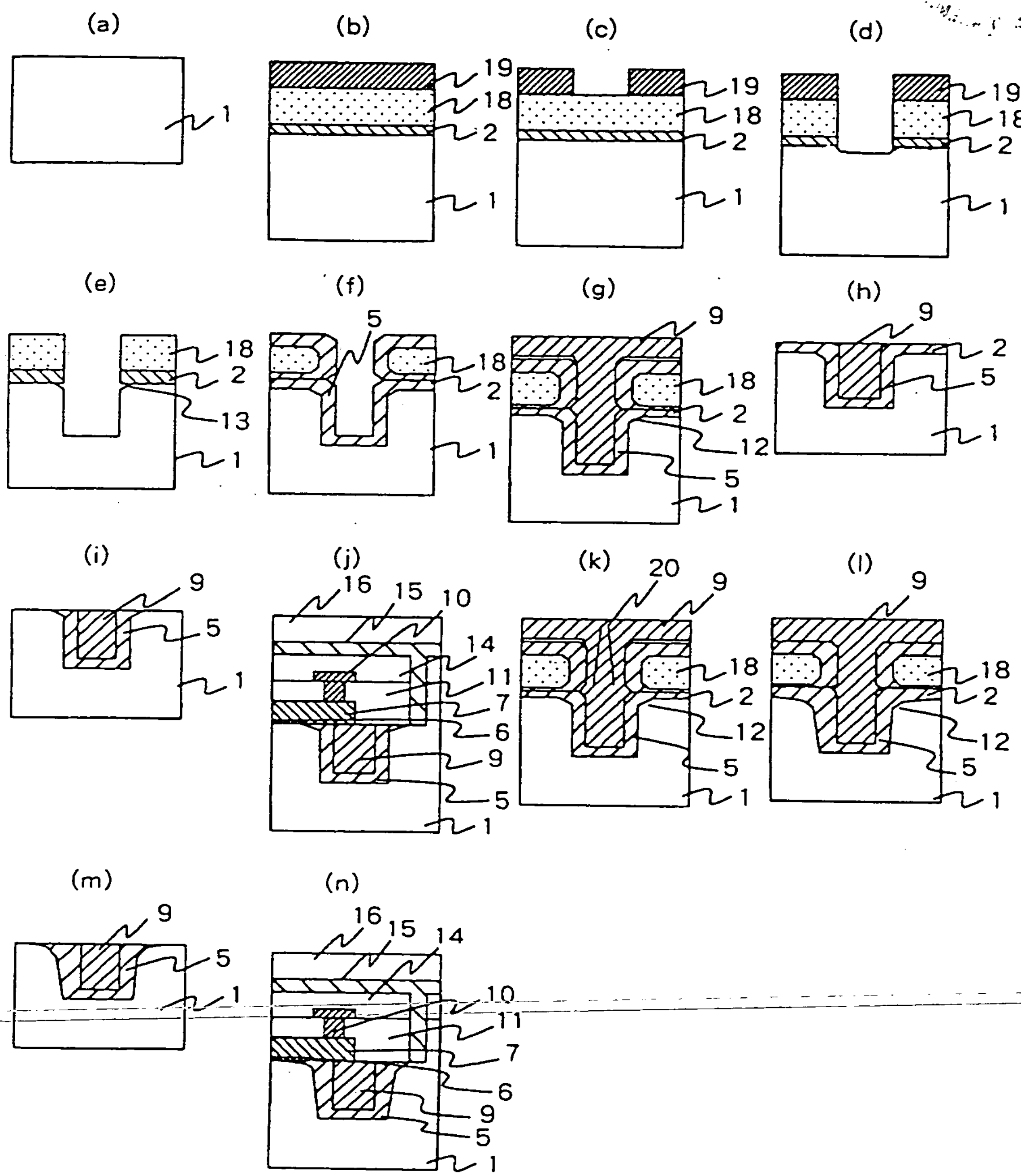
FORMATION OF INTER-LAYER INSULATING FILM
122

【図4】 [Fig. 4]

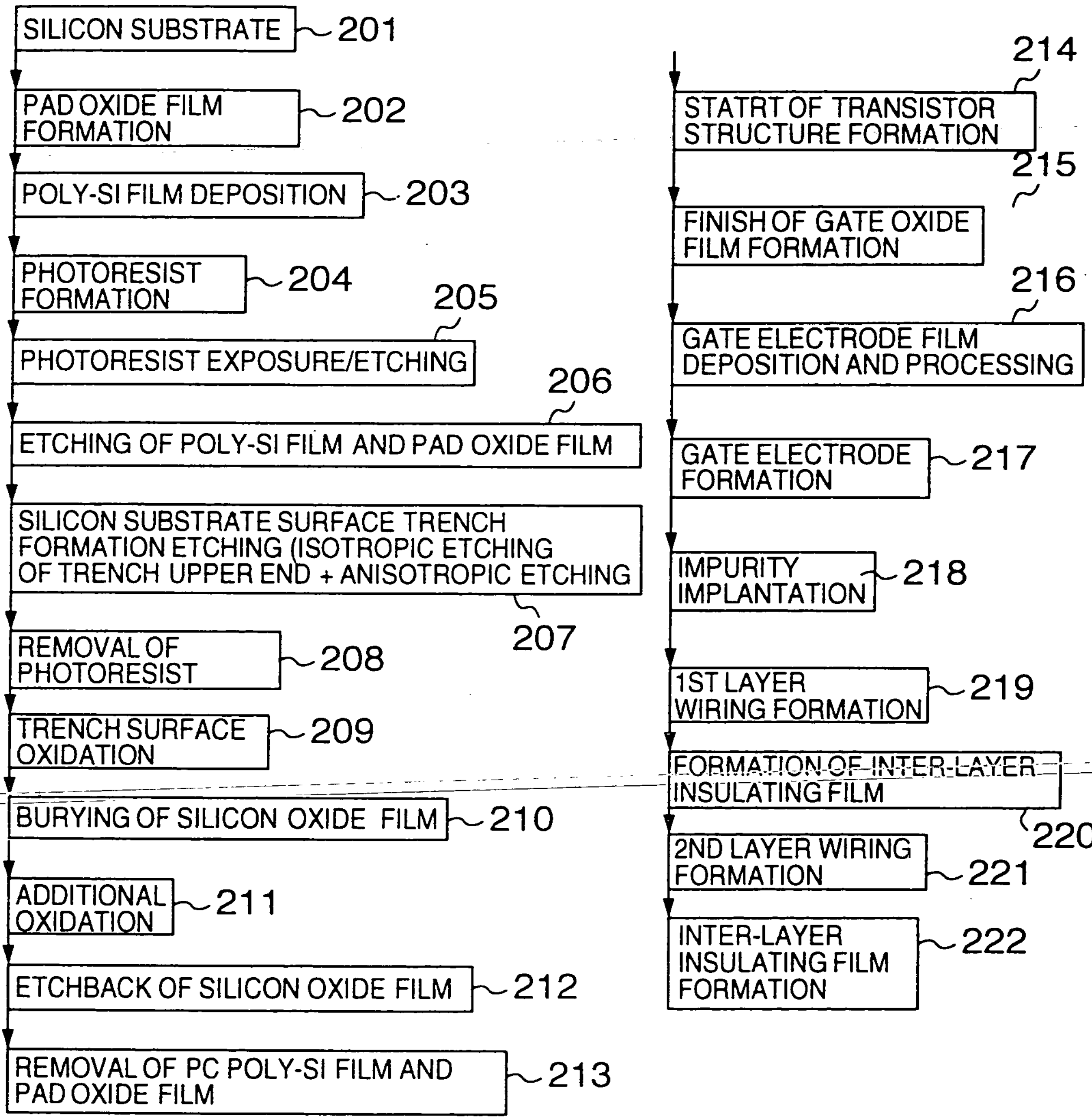
Fig.4

図 4



[Fig. 5]

FIG. 5



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PHOTORESIST FORMATION
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SILICON SUBSTRATE SURFACE TRENCH FORMATION ETCHING (ISOTROPIC ETCHING OF TRENCH UPPER END + ANISOTROPIC ETCHING
207
REMOVAL OF PHOTORESIST
208
TRENCH SURFACE OXIDATION
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BURYING OF SILICON OXIDE FILM
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2ND LAYER WIRING FORMATION
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INTER-LAYER INSULATING FILM FORMATION
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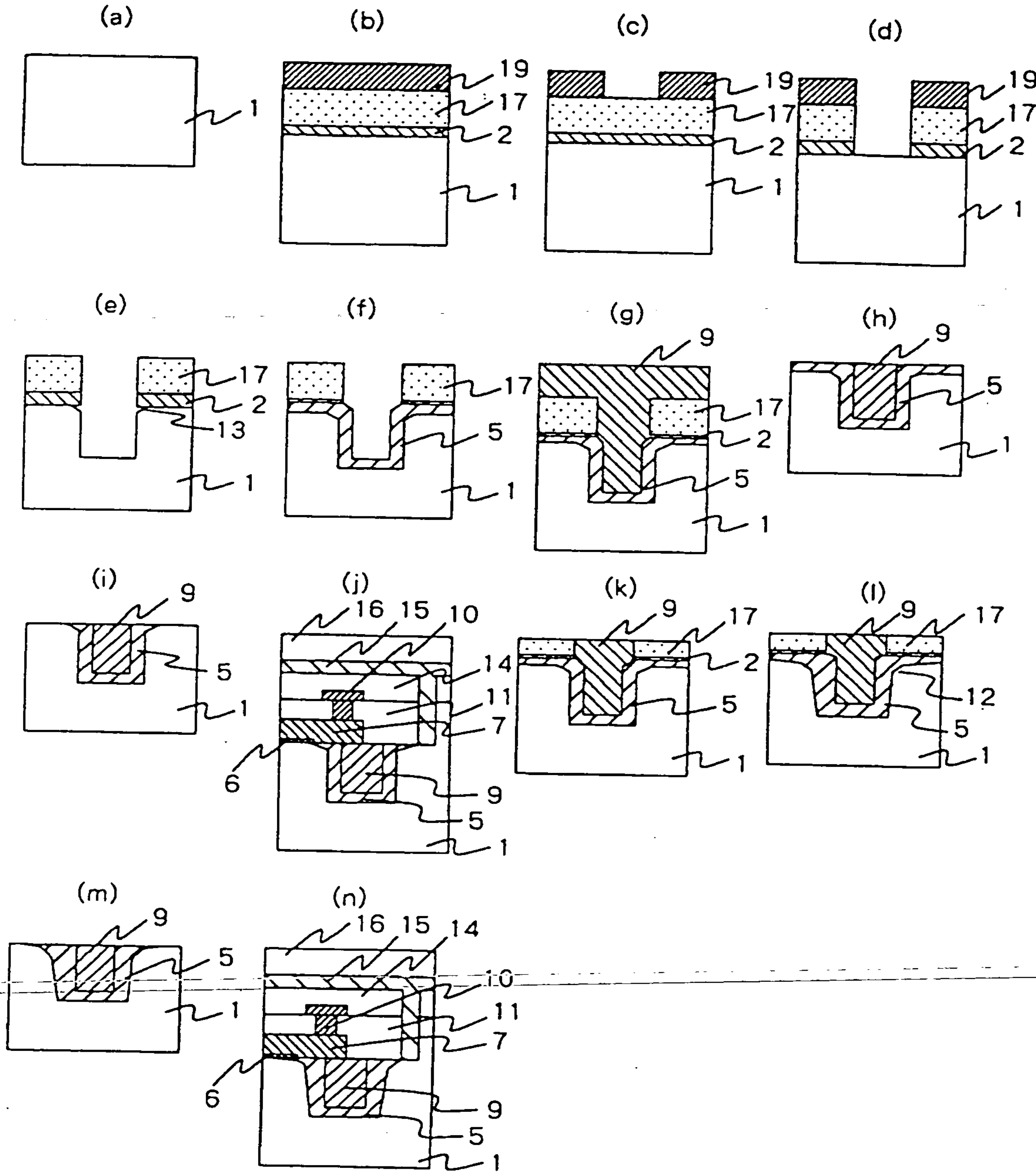
【図６】 [Fig.6]

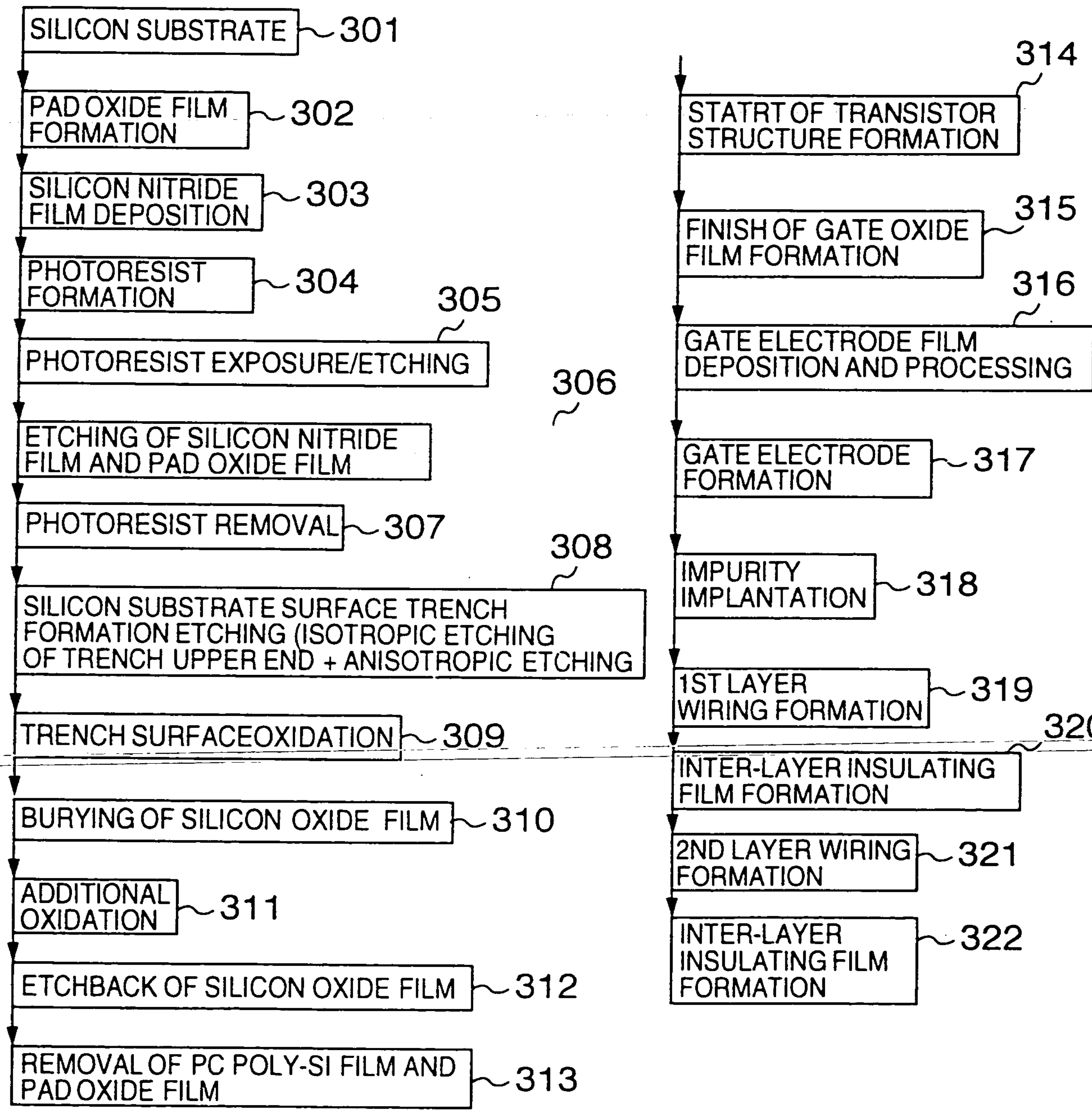
Fig. 6

図 6



[Fig.7]

FIG. 7



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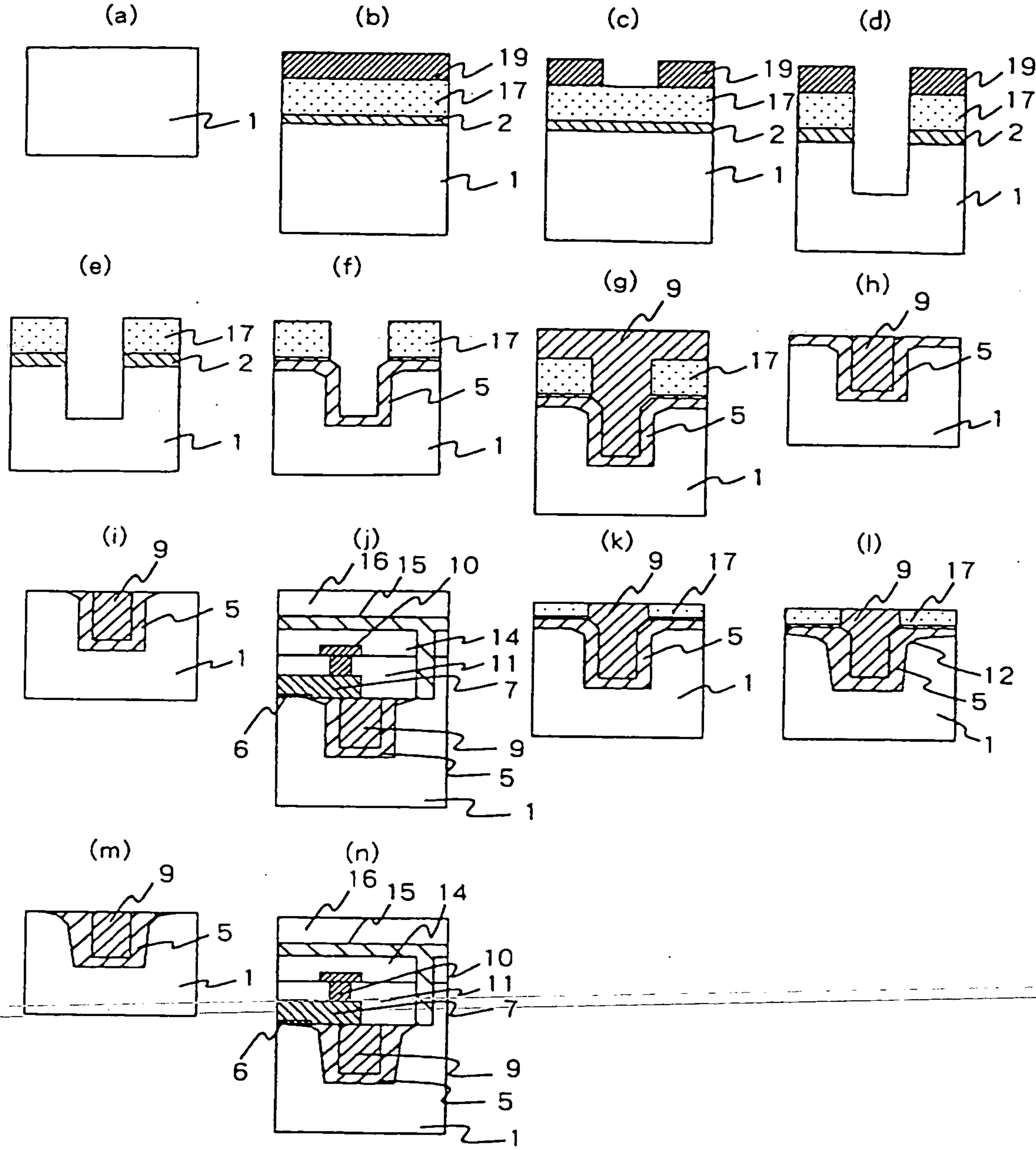
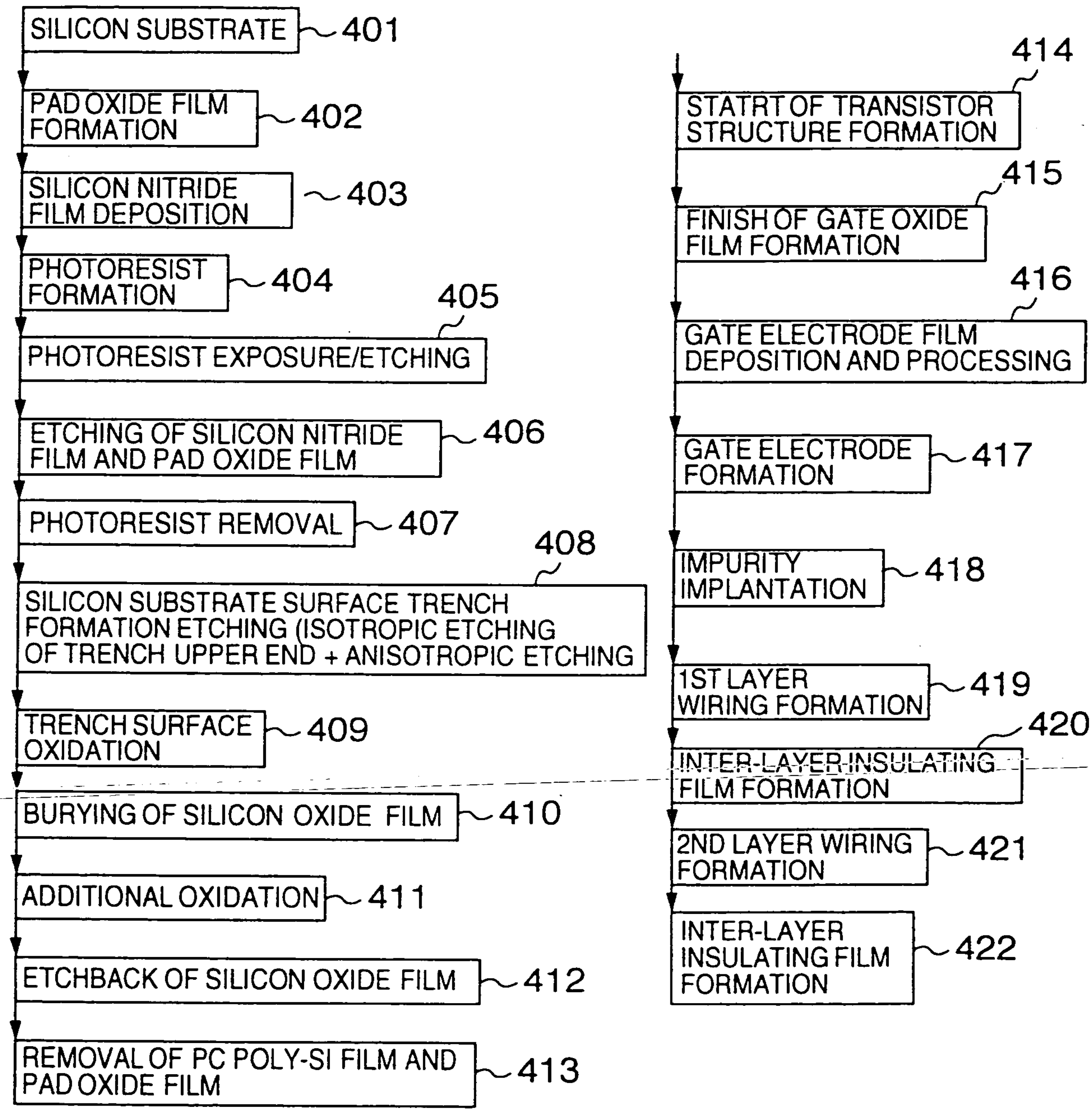
【図8】 [Fig.8]

Fig.8
図 8



[Fig. 9]

FIG. 9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[Title of Document] Abstract

[Abstract]

[Problem] To provide a semiconductor device having a device isolation oxide film structure, and a fabrication method thereof, for preventing the occurrence of the increase of a leakage current of an MOS transistor or the drop of its breakdown voltage characteristics resulting from the field concentration in the proximity of an end portion of a gate electrode film because the shape of a substrate in the proximity of the upper end of a trench for isolating the device becomes an acute angle.

[Solving Means] In a semiconductor device having a trench isolation structure, a trench surface is selectively oxidized by a prior art method, an oxidation prevention film is then removed, the entire surface of the substrate is again oxidized under the state where only the substrate or the oxide film on the trench surface is exposed, and a radius of curvature is provided to the shape of the oxide film in the proximity of the upper end of the trench.

[Selected Drawing] Fig. 3